

Cheating the diffraction limit: electrodeposited nanowires patterned by photolithography

Chengxiang Xiang,[†] Yongan Yang[†] and Reginald M. Penner*

Received (in Cambridge, UK) 8th September 2008, Accepted 6th November 2008

First published as an Advance Article on the web 6th January 2009

DOI: 10.1039/b815603d

The diffraction limit, $d \approx \lambda/2$, constrains the resolution with which structures may be produced using photolithography. Practical limits for d are in the 100 nm range. To circumvent this limit, photolithography can be used to fabricate a sacrificial electrode that is then used to initiate and propagate the growth by electrodeposition of a nanowire. We have described a version of this strategy in which the sacrificial electrode delimits one edge of the nascent nanowire, and a microfabricated “ceiling” constrains its height during growth. The width of the nanowire is determined by the electrochemical deposition parameters (deposition time, applied potential, and solution composition). Using this method, called lithographically patterned nanowire electrodeposition (LPNE), nanowires with minimum dimensions of 11 nm (w) \times 5 nm (h) have been obtained. The lengths of these nanowires can be wafer-scale. LPNE has been used to synthesize nanowires composed of bismuth, gold, silver, palladium, platinum, and lead telluride.

Introduction

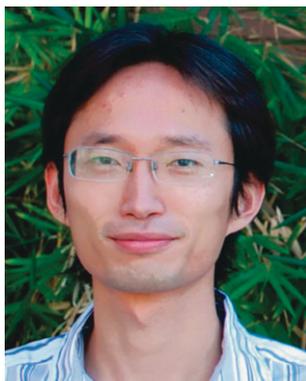
Nanowires are finding applications in an ever expanding list of devices. Among their capabilities, nanowires composed of metals,^{1–8,11–17,19–23,31–34,39,40} semiconductors,^{6–10,18,24–29,41–43} metal oxides,^{30,44–58} and other materials^{59–65} can detect molecules,^{30,45,66,67} process electrical signals as transistors,^{68–77} diodes,^{78–83} and switches,^{84–92} and they can generate,^{79–82} absorb,^{93–95} and detect light.^{96–98} Nanowires can function as

lasers,^{99,100} strain sensors,¹⁰¹ and solar cells.^{93–95,102} Their remarkable utility and versatility is placing a premium on the development of new methods for preparing nanowires. But why are these new methods required?

Copper nanowires, for example, are already extensively used as interconnects deep within some types of integrated circuits, especially microprocessors.¹⁰³ These nanowires are produced using photolithography in conjunction with the damascene or double damascene methods,^{103–105} both of which allow the down-sizing of features produced at or above the diffraction limit of light. The utility of such copper nanowires for applications other than interconnects is limited, however, because these nanowires are embedded in a trench and surrounded on three sides by either silicon or a dielectric.

Department of Chemistry, University of California, Irvine, CA 92697-2025, USA. E-mail: rmpenner@uci.edu;
Fax: +1 949 824 8125; Tel: +1 949 824 8572

[†] These authors contributed equally to this manuscript.



Chengxiang Xiang

Chengxiang Xiang was born in Zhejiang, China, in 1981. He received his BS in modern physics from the University of Science and Technology of China (USTC) in 2004. He joined the Penner research group in 2005. He received his MS in chemical and material physics from the University of California, Irvine, in 2006. He is currently working on the fabrication and characterization of electrochemical memory switching elements.



Yongan Yang

Yongan Yang studied chemistry at NanKai University. In 1999, he earned a PhD from the Institute of Photographic Chemistry, Chinese Academy of Sciences, supervised by Professor Yao. Then he was honored with a Humboldt Fellowship (Germany) during 2000–2002, working with Professor Baumgärtel at Free University, Berlin. Afterwards, he worked as a postdoc with Professor Kern at the Max-Planck-Institute for Solid State Research, Stuttgart, and with Professor Cao at the University of Florida, respectively. He is an Assistant Specialist in the Penner research group. His research interests include functional nanomaterial synthesis and the exploration of their applications in energy conversion and storage.

Table 1 Summary of fabrication methods capable of preparing ultra-long (length > 1 μm) nanowires

Corresponding author	Accessible nanowire composition(s)	Nonlinear nanowires and patterning?	Lateral dimensions	Maximum length	Substrates	Ref(s)
^a Adelung <i>et al.</i>	Metal (Au, Pt, Fe–Co–Ni)	No	< 16 nm	> 3 mm	Glass, Nafion, polyimide, graphite, VSe ₂	1
^b Buriak <i>et al.</i>	Metal (Au, Pd, Pt)	Yes	~ 10 nm	> 100 μm	Silicon	2–4
^c Gösele <i>et al.</i>	Metal (Au, Ni)	Yes	50–300 nm	Wafer scale	Silicon	5
^d Heath <i>et al.</i>	Metal (Al, Au, Cr, Nb, Ni, Pt, Ti), semiconductor (Si)	No	8 nm	> 2–3 mm	Silicon, PDMS	6–8
^e Lee <i>et al.</i>	Semiconductor (Si)	No	18–46 nm	1.5–2 mm	Silicon	9
^f Lieber <i>et al.</i>	Semiconductor (Si)	No	20–80 nm	> 2 mm	Silicon	10
^g Jorristma <i>et al.</i>	Metal (Au, Pd, Ta, Ni)	No	20–120 nm	1 cm	InP(001)	11, 12
^h Murphy <i>et al.</i>	Metal (Ag, Au)	No	30–40 nm	12 μm	Free standing	13–15
ⁱ Natelson <i>et al.</i>	Metal (Au, Pd)	No	3 nm	> 1 μm	GaAs/AlGaAs	16, 17
^j Noda <i>et al.</i>	Semiconductor (Si)	No	80–100 nm	2–3 mm	Silicon/quartz	18
^k Whitesides <i>et al.</i>	Metal (Au)	Yes	20 nm \times 50 nm	Millimetre range	Glass/silicon	19, 20
^l Xia <i>et al.</i>	Ag	No	30–40 nm	10 ~ 50 μm	Free standing	21–23
^m Penner <i>et al.</i>	Metal (Au, Ag, Cu, Mo, Ni, Pd, Sb), semiconductor (Bi ₂ Te ₃ , Ag ₂ O, CdSe, CdS, MoS ₂ , MoO ₂)	No	10 nm–1 μm	> 100 μm	Highly oriented pyrolytic graphite (HOPG)	24–34
ⁿ Penner <i>et al.</i>	Metal (Au, Ag, Bi, Pd, Pt), semiconductor (Bi ₂ Te ₃ , CdTe, PdTe)	Yes	5 nm \times 11 nm	Wafer scale	Glass, silicon, Kapton	35–38

^a Formation of nanowires within cracks in a thin film. ^b Acid stimulated metal nanowire formation in self-assembled monolayers of aligned, horizontal block copolymer cylinders. ^c Templated electrochemical deposition of nanowires using laser interference lithography (LIL). ^d Superlattice nanowire pattern transfer (SNAP). ^e Thermal evaporation of SiO powder. ^f Nanocluster-catalyzed vapour–liquid–solid (VLS) growth using Si₂H₆ reactant. ^g Metal deposition at an angle onto V-grooved InP substrate created by holographic laser interference lithography and anisotropic etching. ^h Self nucleation and growth *via* metal ions' reduction in solution phase. ⁱ Metal deposition into nanometre-scale stencils formed by molecular-beam epitaxy (MBE). ^j Thermal evaporation of pre-sintered Si powder under normal pressure. ^k Nanoskiving: combination of thin film deposition and ultramicrotome sectioning. ^l Nanoparticle-mediated anisotropic growth *via* Ostwald ripening in solution phase. ^m Electrochemical step edge decoration (ESED). ⁿ Lithographically patterned nanowire electrodeposition (LPNE).

“Exposed” metal nanowires can be patterned on top of glass or silicon surfaces by using electron beam lithography (EBL) in which an electron beam serially exposes a photoresist layer with very high resolution. EBL is widely used for patterning nanowires for research and development applications but it has not seen wider use because of its intrinsic

inefficiency: Each nanowire must individually be “written” with an electron beam that moves, typically, at a speed of 10 cm h⁻¹.¹⁰⁶

In order to expedite the assimilation of nanowires into various technologies, two barriers must be overcome: first, it must be possible to efficiently synthesize ultra-long nanowires ($L > 100 \mu\text{m}$) that possess a high degree of diameter uniformity and that are free from breaks, and second, it must be possible to exercise control over the location and two-dimensional trajectory of a nanowire on a surface. Fabrication methods that satisfy either of these two criteria are listed in Table 1 and it is apparent here that very few nanowire fabrication methods presently satisfy both.

In 2005, a graduate student in our laboratory, Erik Menke, discovered a new approach to nanowire fabrication in which photolithography was first used to pattern an evaporated nickel film deposited on a glass microscope slide. Without removing the photoresist required for the patterning process, the nickel edge exposed at the perimeter of the patterned region was used to electroplate a metal (Pt, Au, or Pd) nanowire from an aqueous solution of the corresponding ion. Finally, the photoresist and the patterned nickel layer were both removed leaving the electrodeposited nanowire on a glass surface (Fig. 1). This approach enabled nanowires that were millimetres in total length to be lithographically patterned onto glass surfaces—a capability that we found very

**Reginald Penner**

Irvine, in 1990. His research group investigates the properties of nanomaterials prepared by electrodeposition, and develops new technologies based upon these nanomaterials. He also directs the School of Physical Sciences Center for Solar Energy.

Reginald Penner studied chemistry and biology at Gustavus Adolphus College in St. Peter, Minnesota, graduating in 1983, and he earned a PhD in chemistry from Texas A&M University in 1987, working with Professor Charles R. Martin. He held postdoctoral appointments at Stanford and Caltech, working with Professor Nate Lewis, before joining the chemistry faculty at the University of California,

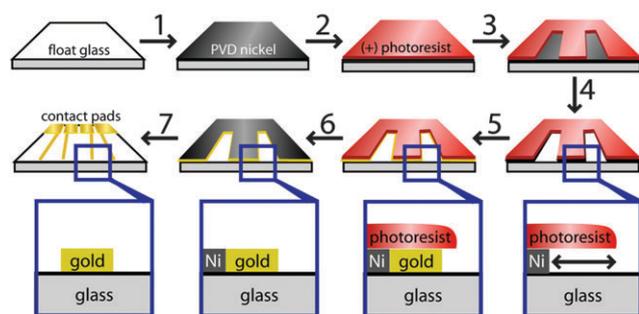


Fig. 1 Process flow for the formation of gold nanowires using the seven-step LPNE method. Reproduced with permission from *Nature Materials*, 2006, 5, 914–919. Copyright 2006 Nature Publishing.³⁶

exciting. But Erik also noticed something unexpected: in some initial trials, gold nanowires prepared using this method were flat. Erik recognized that this was caused by the undercutting of the photoresist during the initial nickel removal step (Fig. 1, step 5). This undercutting caused the formation of a rectangular “trench” at the edges of the patterned region into which the nascent nanowire was deposited. The nanowire electrodeposited within this trench was flat and it had a uniform thickness that matched the thickness of the evaporated nickel layer. Subsequently, Erik showed that this undercut could be intentionally and reproducibly formed by controlled “over etching” of the nickel layer thereby affording him precise control of the nanowire height. Erik’s method was refined by students Chengxiang Xiang and Michael Thompson and their data formed the basis of our first publication describing the lithographically patterned nanowire electrodeposition (LPNE) method in 2006.³⁶

Since then, we have been interested in defining the limits of the LPNE method and in expanding these limits. In this feature article, we summarize the new capabilities of the LPNE method that have emerged over the past three years.

The LPNE method

(a) Process flow for wire fabrication

The lithographically patterned nanowire electrodeposition (LPNE) method involves seven steps (Fig. 1). In step 1, a sacrificial film of either nickel or silver is deposited by physical

vapor deposition (PVD) at a rate of $0.5\text{--}1.5 \text{ \AA s}^{-1}$. This metal layer is 5–200 nm in thickness and it defines the ultimate thickness of the nanowire that will be produced. In step 2, the metal film is over-coated with a uniform layer of a positive photoresist (PR) (Shipley 1808) using spin-coating (step 2). This PR layer is “soft baked” at $90 \text{ }^\circ\text{C}$ for 30 min and cooled to room temperature. In step 3 of the LPNE process the PR layer is patterned by exposing it for 1.5 s using 365 nm light through a contact mask. In our lab, the light source is an intense NUV illumination system (Model 97434 Newport Corporation) controlled by a digital exposure controller (Model 68945 Newport Corporation). This level of sophistication is not required, however, and we have successfully prepared nanowires using contact masks prepared by laser printing onto transparency film in conjunction with a hand-held UV lamp. It is important to note here that we routinely carry out this photolithography in a standard chemistry laboratory with unfiltered air. Pattern transfer to the PR layer is completed by developing the exposed PR using Shipley MF-319 for 20 s, followed by rinsing in pure water, and drying in a stream of N_2 or compressed air. Now, in step 4, the exposed metal layer is removed and an undercut is produced at the perimeter of the exposed region. For a nickel layer, 0.8 M nitric acid is used for this purpose whereas for silver the etchant is 18% NH_4OH and 4% H_2O_2 . The etching time is adjusted by trial and error to produce a $\approx 300 \text{ nm}$ undercut and it varies depending on the thickness of the metal layer. At this point, a lithographically patterned, recessed metal edge has been produced on the glass surface. In step 5, we electrodeposit the nanowire into this “horizontal trench”. For metals, including gold, palladium, platinum, or bismuth, electrodeposition can be carried out potentiostatically and the wire width is then related to the concentration of metal ion in the plating solution, the deposition potential, and the deposition time. For lead telluride, a more complex procedure, described later, is required. The electrochemical cell employed for nanowire growth is a simple, 50 mL, one compartment, three-electrode cell. The composition of plating solutions, and other electrodeposition parameters are summarized in Table 2. A saturated calomel reference electrode (SCE) and a 2 cm^2 Pt foil counter electrode were also employed. The final two steps, 6 and 7, involve the removal of the PR layer and the sacrificial metal electrode. The photoresist is removed first by rinsing with electronic grade acetone (Acros), methanol (Fisher), and

Table 2 Electrodeposition conditions for synthesizing nanowires of Au, Pd, Pt, Bi and PbTe

Material	Electrodeposition solution (all solutions are aqueous)	Deposition method	Deposition potential/V vs. SCE	Deposition time	Minimum wire width
Au	6 mM AuCl_3 (Clean Earth Solutions, Carlstadt, NJ)	Potentiostatic	$-1.00\text{--}(-0.85)$	20–500 s	11 nm
Pd	0.1 M KCl; 0.2 mM PdCl_2	Potentiostatic	0.15–0.22	10–400 s	44 nm
Pt	0.1 M KCl; 1.0 mM K_2PtCl_6	Potentiostatic	$-0.10\text{--}0.05$	100–500 s	47 nm
Bi	1 mM $\text{BiNO}_3 \cdot 5\text{H}_2\text{O}$; 20 mM boric acid; 20 mM tartaric acid; 20 mM NaCl; 10 mM K_2SO_4 ; 3 mM glycerol; 0.07 M HNO_3 ; 1.2% gelatin	Potentiostatic	-0.115	50–200 s	54 nm
PbTe	83 mM $\text{Pb}(\text{NO}_3)_2$; 0.83 mM TeO_2 ; 92 mM EDTA; pH = 10	Potentiodynamic	$-0.85\text{--}(-0.20)$	1–5 scans at 50 mV s^{-1}	60 nm

finally Nanopure water in sequence. Then in step 7, the metal film is removed using the same etching solution that was used earlier in step 4.

In general, the nanowires produced using the LPNE method adhere strongly to the glass, oxidized silicon, or Kapton surfaces on which they are deposited. Promoting wire adhesion to the surface is a sub-monolayer of the metal (either silver or nickel) that persists on the insulator even after exposure to the etching solution. This residual metal is observable by X-ray photoelectron spectroscopy.

(b) Independent control over lateral wire height and width

An important attribute of the LPNE method is that the nanowire height and width can be independently controlled. The horizontal trench produced in step 4 is the key to control of the nanowire height. This trench has a height that matches that of the recessed nickel layer (Fig. 2). Consequently, the height of the nanowire—that is, its dimension perpendicular to the surface—is controlled by the thickness of the evaporated metal layer deposited in step 1 of the process. A comparison of the thickness of this metal layer and the nanowire height—both measured using atomic force microscopy (AFM)—shows they are identical within our measurement precision (Fig. 2a). The minimum height of the nanowire is in the 5–8 nm range depending on material.

The width of the nanowire is controlled by the electro-deposition duration together with the composition of the plating solution and the applied deposition potential. For the electro-deposition of a material into a rectangular trench using a time-invariant current density, J_{dep} , the width of the deposited nanowire, w , is given by:³⁵

$$w = \frac{J_{\text{dep}} t_{\text{dep}} V_m}{nF} \quad (1)$$

where t_{dep} is the deposition time, V_m is the molar volume of the deposited material, n is the number of electrons required to reduce each metal complex ion, and F is Faraday's constant (96450 C/eq). Scanning electron microscopy (SEM) has been used to measure the nanowire width as a function of deposition time (Fig. 2b). For nanowires composed of metals, the deposition time ranges from 5 to 500 s and the nanowire width increases linearly with the deposition time qualitatively as predicted by eqn (1). The minimum wire width obtainable by LPNE is ≈ 11 nm.

Thus, in the LPNE method, parameters associated with photolithography determine the position and 2D trajectory of the nanowire on the surface, its length and its height. Parameters associated with the electro-deposition control the nanowire width. Importantly, while LPNE makes possible extremely small wires, the distance separating nanowires on the surface continues to be constrained by the optical

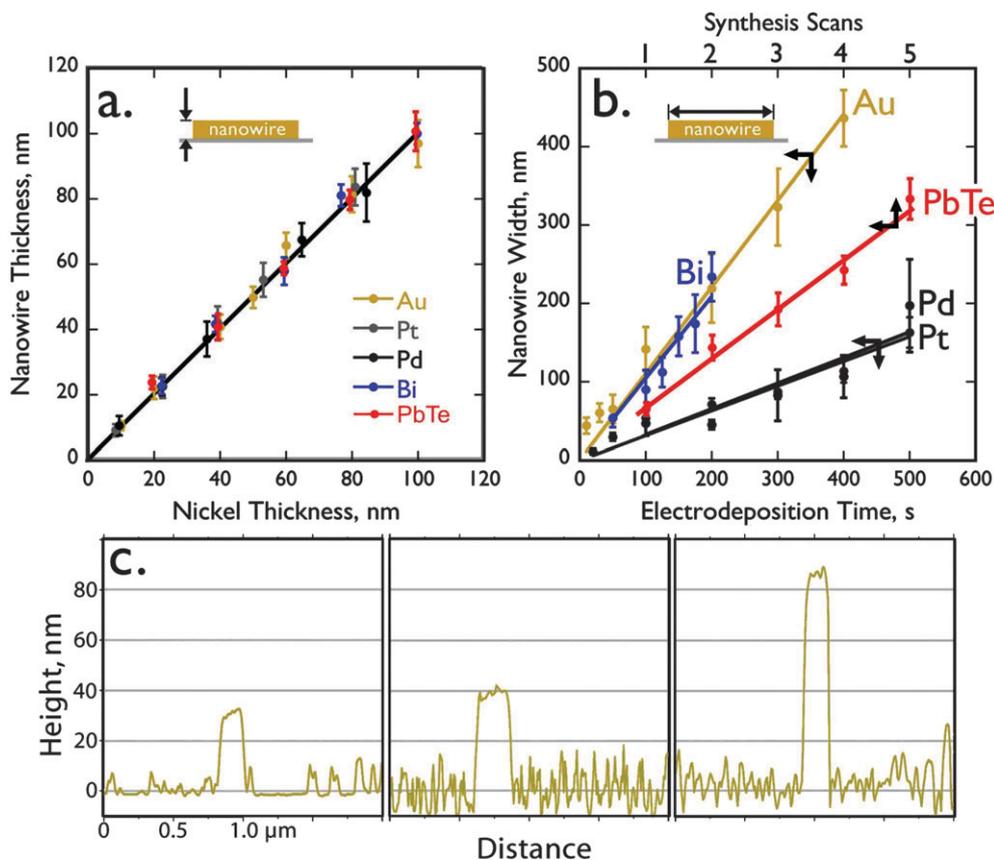


Fig. 2 Both the height and the width of a nanowire produced by LPNE can be independently controlled. (a) Nanowire height measured by atomic force microscopy (AFM) versus the thickness of the evaporated nickel or silver layer. (b) Nanowire width measured by scanning electron microscope versus electro-deposition duration. The composition of the plating solution is as indicated in Table 2. (c) Nanowire cross-sectional profiles measured by AFM. Reproduced with permission from *ACS Nano*, 2008, 2, 1939–1949. Copyright 2008 American Chemical Society.³⁵

diffraction limit. A practical limit for this interwire “pitch” in our laboratory is presently 2 μm .

Metal nanowires

(a) The electrochemistry of LPNE nanowire growth

Nickel is employed as the sacrificial electrode because it can be selectively removed by nitric acid without damaging gold, palladium, or platinum. Silver is substituted for nickel in the case of bismuth nanowire growth because it can be selectively removed using a mixture of NH_4OH and H_2O_2 whereas the HNO_3 required for removal of the nickel layer also attacks bismuth.

The properties of the nanowire electrodeposition depend both on the composition of the sacrificial electrode and on the composition of the plating solution. In the LPNE experiment, the electrode consists of an edge of exposed metal—a “nanoband” electrode—that wraps around the perimeter of the lithographically pattern region. Cyclic voltammetry (CV) can be used to study the electrochemistry in four metal plating solutions at this nanoband electrode. Two distinctly different behaviors are seen in the data shown in Fig. 3: if one looks first at the nickel edge data of Fig. 3a–c, the first metal deposition scan shows something unusual: the deposition current after the scan reversal at the negative limit is greater than before it for all three metals in spite of the fact that the concentration of metal ions near the nanoband is being depleted on the forward scan. The reason for this unusual voltammetric behavior

derives from the fact that the nickel edge is oxidized and it is unable to efficiently transfer electrons to metal ions within the trench. As the metal deposition reaction proceeds, however, the NiO surface is replaced with gold (Fig. 3a), palladium (b) or platinum (c), all of which catalyze electron transfer and resist oxidation. Continued growth of the deposition current for all three metals is observed on subsequent scans as the replacement of NiO with noble metal is completed.

Bismuth deposition at a silver edge (Fig. 3d) shows dramatically different behavior, with the deposition current decreasing both on the first voltammetric scan and on subsequent scans. Here, in contrast to the case with nickel, the silver edge does not impede electron transfer because it does not support the formation of a significant oxide overlayer at this pH. The electrodeposition of bismuth has the opposite effect: instead of catalyzing electron transfer, electrodeposited bismuth is highly resistive and the ohmic drop within it reduces the overpotential available for continued bismuth deposition by dissipating some of this overpotential as heat. In addition, bismuth is a much poorer electrocatalyst than silver, a factor that contributes to the attenuation in the deposition rate as a function of time seen in Fig. 3d.

In spite of the differences seen in the details of the electrodeposition process at nickel and silver nanobands, nanowires of all four metals are readily obtained by potentiostatic growth under the conditions indicated in Table 2. This means that the LPNE method is remarkably tolerant of variations in the microscopic properties of the electrodeposition reaction. This versatility extends to the growth by LPNE of nanowires composed of semiconductors, such as lead telluride, a material which we shall discuss in some detail below. Subject to the constraint that the final etching step selectively removes the sacrificial metal layer, LPNE seems to be a materials-general method for patterning electrodeposited materials as nanowires.

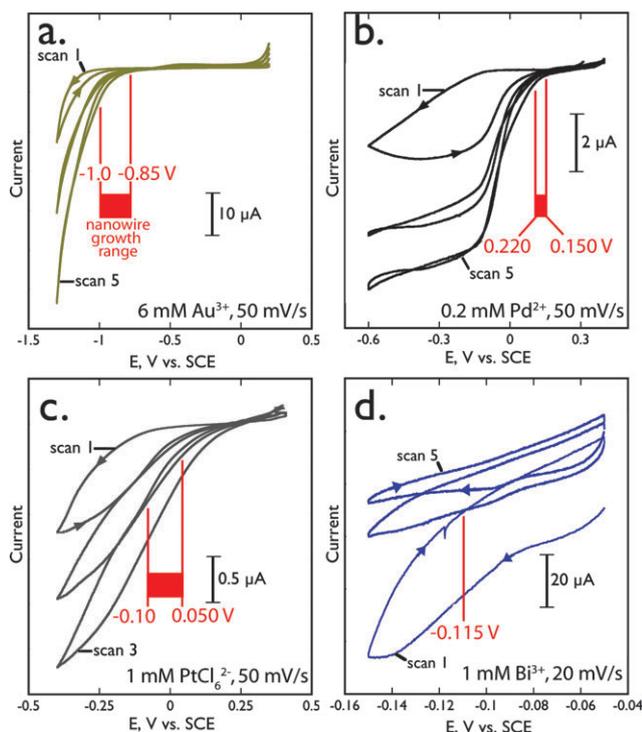


Fig. 3 Cyclic voltammograms acquired in different metal plating solutions: (a) gold, (b) palladium, (c) platinum, (d) bismuth. The ranges of electrodeposition potentials are indicated in red. Reproduced with permission from *ACS Nano*, 2008, 2, 1939–1949. Copyright 2008 American Chemical Society.³⁵

(b) Nanowire patterning and LPNE process latitude

A distinguishing characteristic of LPNE is its ability to produce nanowires in any two-dimensional pattern subject to the “wire proximity constraint”: Sections of a single wire cannot approach one another at a distance below the diffraction limit, and no two nanowires produced in a single LPNE patterning operation can be positioned closer than this limit, which is approximately 2 μm in our laboratory.

Examples of nanowire patterns that can be obtained in a single LPNE patterning operation are shown in Fig. 4a–d. In these patterns, the critical dimension for the lithography that was performed is in the 10 μm range. The widths of the squares shown in the pattern of Fig. 4d, for example, are constrained by the diffraction limit. The continuous length of the nanowires contained within these patterns can easily exceed 1 mm. The parallel gold nanowires of Fig. 4b, for example, are spaced by 9 μm and are 1 cm in length. The gold nanowire shown in the spiral pattern in Fig. 4c has a total length of 2.7 cm (the patterned area is 0.5 mm \times 0.5 mm).

The length of these ultra-long nanowires can be reduced by appending a second photolithography step to strip away sections of nanowires, as shown in Fig. 4e and f. Here, a

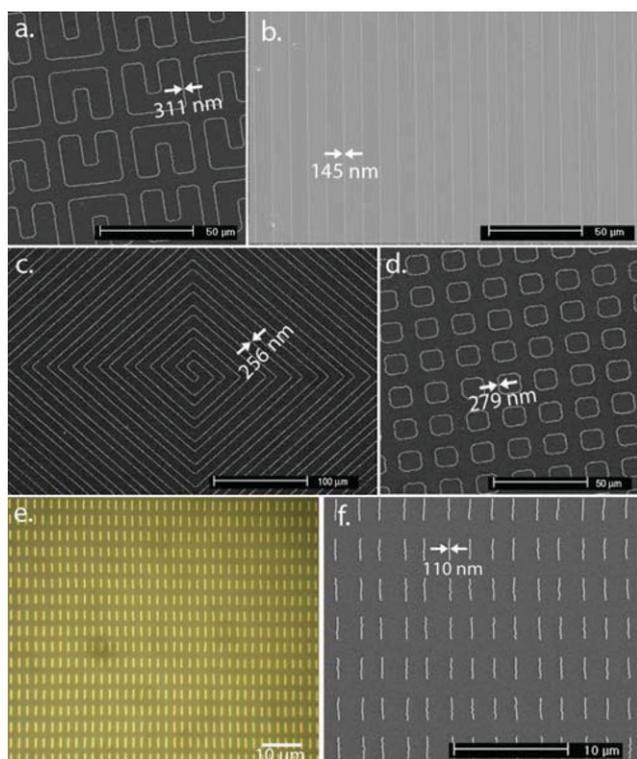


Fig. 4 Scanning electron micrographs (a–d and f) and a photomicrograph (e) of patterned gold nanowires produced using the LPNE method.

parallel array of gold nanowires was “diced” into gold nanorods by masking these wires with 2 μm wide photoresist stripes. The exposed gold segments were then removed by dissolution in an iodide/tri-iodide etching solution (16 mM KI_3 and 8 mM KI). Gold nanorods were revealed after the removal of the photoresist.

The “wire proximity constraint” imposed by the diffraction limit is relaxed when the LPNE process is repeated twice in succession. Using this trick, nanowire patterns can be overlaid on top of one another to form more complex nanowire architectures.

For example, arrays of crossed nanowire junctions can be fabricated by patterning a parallel array of linear metal nanowires using a first LPNE operation, then repeating the entire LPNE process using the same mask rotated by 90° . SEM images of surfaces prepared using exactly this process are shown in Fig. 5. Importantly, the nanowire–nanowire junctions formed in these “LPNE nanowire overlays” have a resistance that is much smaller than that of typical nanowire connecting segments (Fig. 5c).

We have also demonstrated that nanowires can be directly patterned onto flexible Kapton polymer films. Kapton films were cleaned in acetone and pure water and then cut into 2.54 cm \times 2.54 cm squares. These squares were then affixed to a glass slide to facilitate the LPNE processing steps, and released from this surface at the end of the fabrication procedure, which is otherwise identical to the process used for preparing metal nanowires on glass or oxidized silicon. Gold nanowires produced on Kapton (Fig. 6) adhered strongly and maintained their electrical continuity even after repetitive bending of the film.

Finally, we have discovered a method for obtaining, in a single LPNE operation, nanowires that are modulated in height. Shown in Fig. 7a, for example, is a gold “zig-zag” nanowire in which segments of the wire alternate between 22 nm and 78 nm in height (Fig. 7f).

These nanowires are obtained by preparing a sacrificial nickel layer that has the desired height modulation. Height modulated nickel layers were prepared by photopatterning a photoresist layer on a planar nickel film and then evaporating nickel a second time onto this patterned photoresist. After lift-off, a height modulated nickel film is produced as a nanowire growth template. Finally, this height modulated nickel layer is patterned, and nanowire arrays are electrodeposited exactly as in the normal LPNE process to produce height modulated nanowires mimicking the height profile of this nickel film.

(c) Characterizing metal nanowires prepared by LPNE

Scanning electron micrographs (SEMs) of linear metal nanowires composed of gold, palladium, platinum and bismuth on glass are shown in Fig. 8. These nanowires have a well-defined

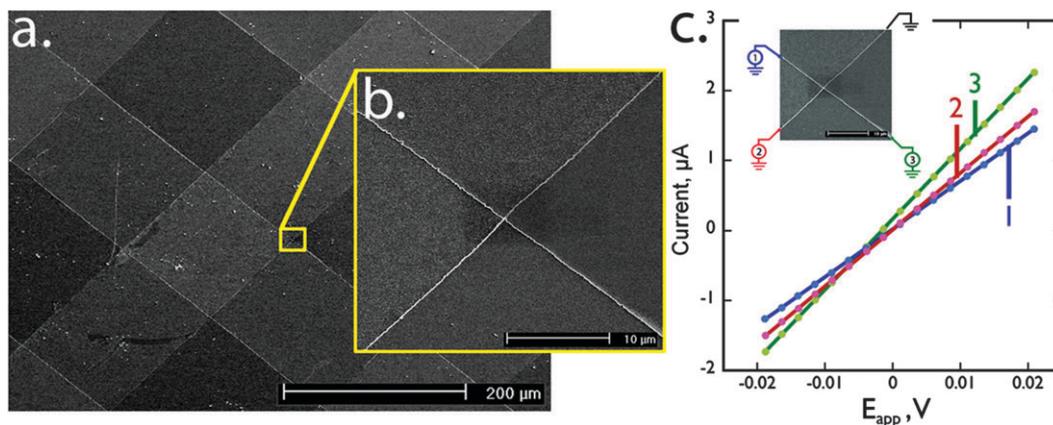


Fig. 5 Crossed gold nanowires prepared by carrying out the LPNE twice in succession (but with rotation of the mask by 90°): (a, b) low and high magnification SEM images of crossed gold nanowires on glass. (c) Current–versus–voltage curves for a typical nanowire–nanowire junction showing I – V curves acquired at three nanowire ends relative to a common ground wire. Reproduced with permission from *ACS Nano*, 2008, 2, 1939–1949. Copyright 2008 American Chemical Society.³⁵

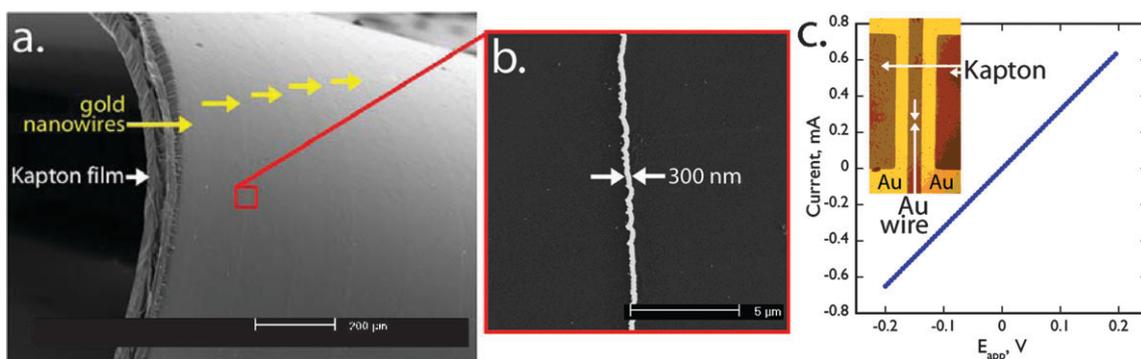


Fig. 6 Gold nanowires on a flexible Kapton film: (a and b) low and high magnification scanning electron micrographs of gold nanowires on a Kapton film. (c) Current-versus-voltage curves acquired using four-point evaporated electrical contacts (insert). Reproduced with permission from *ACS Nano*, 2008, **2**, 1939–1949. Copyright 2008 American Chemical Society.³⁵

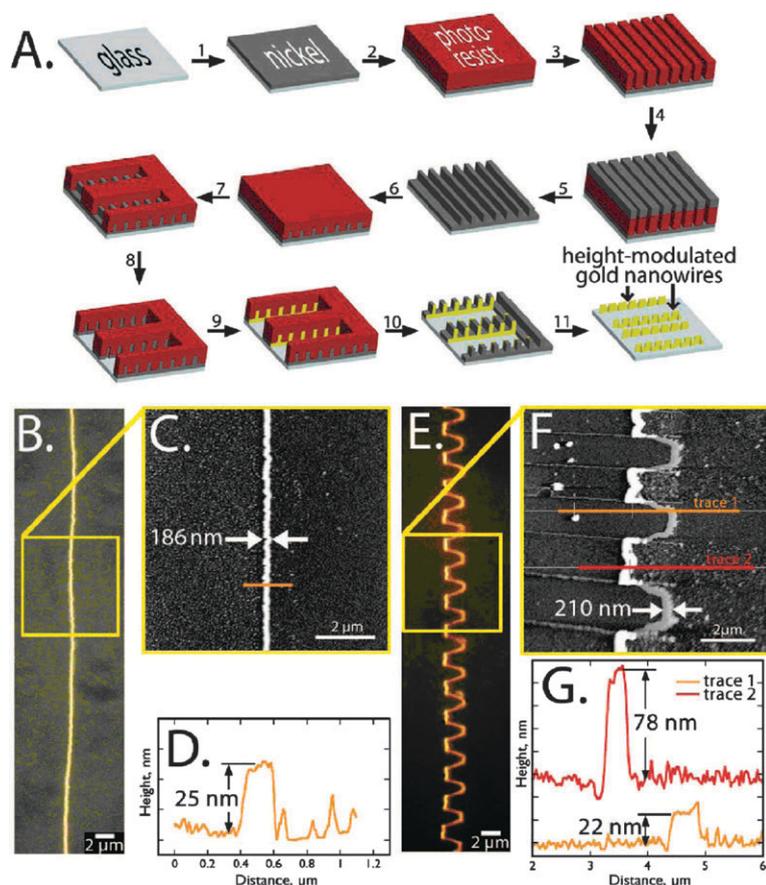


Fig. 7 Fabrication and characterization of gold nanowire types I and II. (A) Schematic of the fabrication method of height modulated nanowires (type II). (B) Dark-field transmission image of wire type I. (C) SEM image of wire type I, and cross-sectional profile (D) as measured with AFM. (E) Dark-field transmission image of wire type II, (F) along with SEM image and (G) AFM cross-sectional profile. Reproduced with permission from *Nano Letters*, 2008, **8**, 2373. Copyright 2008 American Chemical Society.³⁸

and highly uniform width and appear in these images to be continuous and free of gaps for millimetres, in most cases.

These images also expose one type of imperfection in these nanowires—deviations from the straight wire path programmed by the photolithographic mask. Experience has shown that the extent and severity of these “nanowire positioning defects” are mainly a function of the quality of the photolithography operation, including the type of

contact mask employed and whether processing steps were carried out in a cleanroom or (as in Fig. 8) in unfiltered laboratory air. The metal etch carried out in step 4 (Fig. 1) can also cause the path of the metal edge to deviate from the trajectory programmed by photolithographic patterning, but we have concluded that this is a less important contributor to wire positioning defects than the photolithography itself.

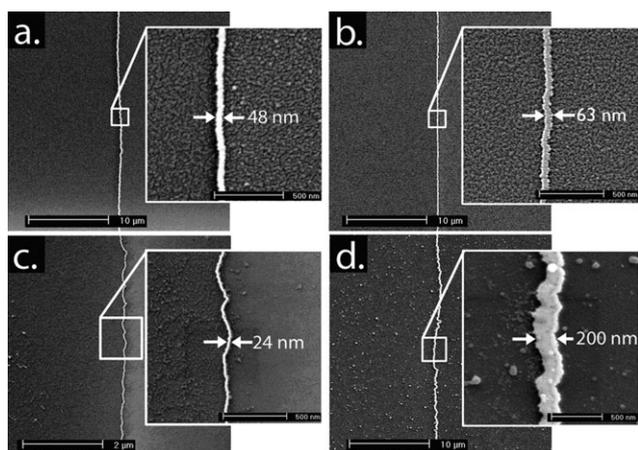


Fig. 8 Scanning electron microscope images of nanowires at two magnifications: (a) gold, (b) palladium, (c) platinum, (d) bismuth. Reproduced with permission from *ACS Nano*, 2008, **2**, 1939–1949. Copyright 2008 American Chemical Society.³⁵

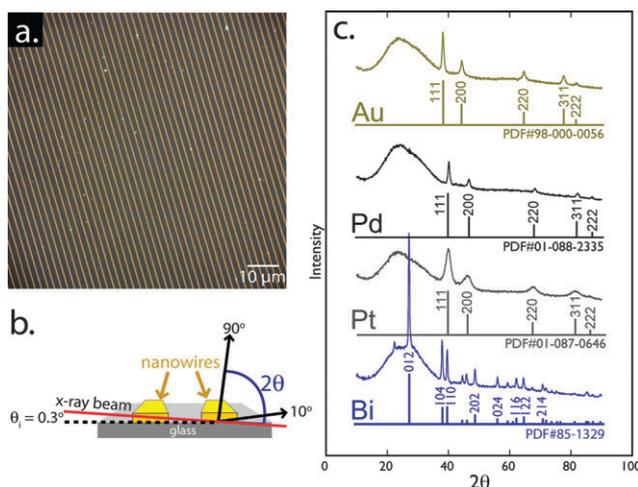


Fig. 9 Characterization of metal nanowires using X-ray diffraction: (a) optical micrograph of an array of linear gold nanowires deposited at 2 μm pitch. (b) Schematic diagram of a GIXRD experiment for nanowire arrays on a glass substrate. (c) X-Ray diffraction patterns for metal nanowire arrays prepared by LPNE. Reproduced with permission from *ACS Nano*, 2008, **2**, 1939–1949. Copyright 2008 American Chemical Society.³⁵

SEM images like those shown in Fig. 8 are used to assess the uniformity of the nanowire height and width. This analysis affords some broad generalizations for different metals as follows: the relative standard deviation RSD_w for the width dimension is lowest for gold ($RSD_{w,Au} = 15\%$) and highest for platinum ($RSD_{w,Pt} = 28\%$). The height dimension is better controlled for all four metals, with RSD_h ranges from $RSD_{h,Bi} = 6\%$ to $RSD_{h,Pd} = 14\%$.

The ability of LPNE to produce dense arrays of nanowires makes possible the use of X-ray powder diffraction to determine the crystallographic structures of nanowires prepared by LPNE. Arrays of thousands of nanowires of 1 cm length and 2 μm in space are used to carry out powder X-ray diffraction measurements using grazing incidence X-ray diffraction (GIXRD, Fig. 9). In the cases of gold, platinum and

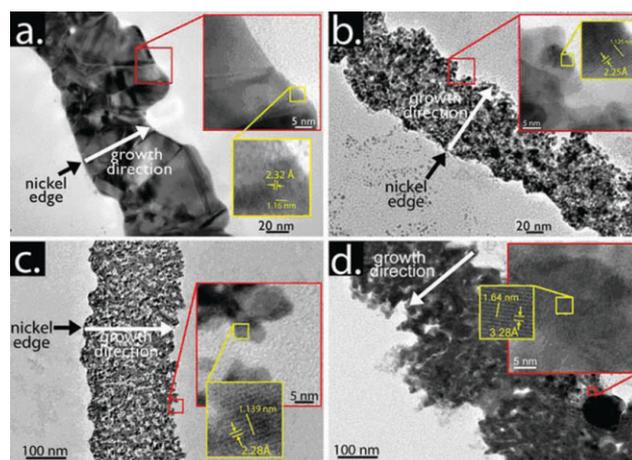


Fig. 10 Transmission electron micrographs (TEMs) showing high resolution lattice fringes (insert): (a) gold, (b) palladium, (c) platinum, (d) bismuth. Nanowire growth directions are indicated by white arrows. Reproduced with permission from *ACS Nano*, 2008, **2**, 1939–1949. Copyright 2008 American Chemical Society.³⁵

palladium, the observed diffraction peaks can be indexed to the face-center cubic (fcc) structure except the broad peak centered at 25° that is produced by diffuse diffraction from the glass surface on which these nanowires were supported. For bismuth nanowires, more than twelve reflections can be indexed to the rhombohedral space group, indicating that the material is highly crystalline.

The nanowires prepared by the LPNE method are polycrystalline and XRD can provide an estimate of the mean grain size based upon Scherrer line broadening if the contribution of strain to the total line broadening can be assumed to be negligible. For nanowire arrays like the one shown in Fig. 9a, the GIXRD experiment produces a scattering vector oriented from 0° to 45° versus surface normal so it is mainly the out-of-plane grain structure that is probed using this method.

In addition to XRD, transmission electron microscopy (TEM) can be carried out together with selected area electron diffraction (SAED) in order to probe the grain structure of nanowires. In general, only the wire height is small enough—between 5 and 20 nm—to enable the transmission of electrons so it is the in-plane grain structure of the nanowires that can be probed using TEM. This means that the grain size information gleaned from TEM is complementary to that provided by XRD, not redundant to it. Sample preparation for TEM usually involves the removal of nanowires from a glass or photoresist-covered surface and the collection of these nanowires onto carbon-coated TEM grids. TEM images (Fig. 10) show the in-plane grain diameters for four metals ranges from 3.9 ± 0.3 nm for bismuth to 40 ± 10 nm for gold. The spacing of the $\{111\}$ lattice plane for all four metals is measured by high resolution TEM (HRTEM) and in all four cases this spacing matched literature values (Fig. 10).

(d) Electrical characterization of metal nanowires

The ability of metal nanowires to conduct current is central to many of their projected applications. However, little electrical

characterization data is available for metal nanowires prepared using the state-of-the-art methods summarized in Table 1, in large measure because these methods are very new and these data have not yet been collected. In fact, there is surprisingly little data on electrical conduction in metal nanowires prepared by EBL or conventional silicon micro-fabrication methods, such as the damascene and double damascene methods. Gold nanowires prepared by EBL have been studied by Durkan and Welland¹⁰⁷ while copper^{104,105,108,109} and tungsten¹¹⁰ nanowires prepared using a variant of the damascene method have been studied by Steinhoggl and co-workers.^{104,105,108–110} Palladium nanowires prepared using a pore-templated electrodeposition process and individually contacted using a focused ion beam (FIB) method have been studied by Marzi and co-workers.¹¹¹

We have investigated the electrical properties of metal nanowires in some detail both at ambient temperature and as a function of temperature to 20 K in order to learn whether LPNE nanowires behave in accordance with the known physics of conduction in nanowires. For bulk metals, the resistivity arises from the scattering of conducting electrons by lattice vibrations and impurity sites. Two additional mechanisms of dissipation contribute to the resistivity of a polycrystalline nanowire: (1) surface scattering and (2) grain boundary scattering. In surface scattering, the specularity coefficient, p , describes the fraction of electrons that is specularly scattered at the wire surface from Fuchs–Sondheimer theory.^{112,113} In grain boundary scattering, the reflection coefficient, R , describes the fraction of electrons that are scattered by the potential barrier at grain boundaries from Mayadas–Shatzkes theory.¹¹⁴

We have been able to measure the values of p and R for nanowires of gold and palladium using equations for the temperature-dependent resistance of nanowires with rectangular cross-sections derived by following the seminal work of Steinhoggl and co-workers who have studied nanowires composed of copper^{104,105,108,109} and tungsten.¹¹⁰ These measurements reveal that the additional resistivity seen in nanowires of Au and Pd derives first and foremost from enhanced grain boundary scattering (Au: 74.1–82.0%; Pd: 46.4–51.7%) and secondarily, from enhanced surface scattering (Au: 6.42–7.87%; Pd: 1.16–2.04%).

Using ultra-long gold nanowires prepared by LPNE, we have studied the effect on the electrical resistance of the electrochemical growth of an oxide monolayer.¹¹⁵ The electrical resistance of gold nanowires was measured as a function of the applied potential while sections of these wires were immersed in a 0.10 M solution of sulfuric acid, and the voltage range investigated coincided with the formation of an oxide monolayer. For the smallest wires investigated in this study, with dimensions of 18 × 95 nm, the growth of 0.8 monolayers of oxide caused the resistance to increase by 57% relative to the resistance of the reduced nanowire. The magnitude of this resistance increase is much larger than can be explained based upon either a simple depression of the specularity parameter, p , or a reduction in the cross-section of the wire (Fig. 11c). As the height of the nanowire increases from this 18 nm minimum value, the induced oxide monolayer causes a progressively smaller resistance elevation (Fig. 11b and c). Based on these

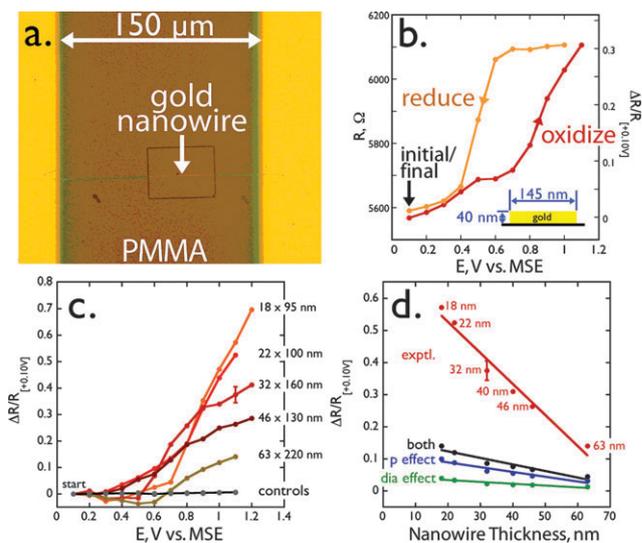


Fig. 11 (a) Photomicrograph showing a gold nanowire bridging two (of four) gold electrodes. (b) Resistance, R , vs. E_{app} for a 40 × 145 nm gold nanowire in 0.10 M H_2SO_4 . (c) $\Delta R/R_{0,1V}$ vs. E_{app} for the oxidation of five other gold nanowires. (d) Plot of $\Delta R/R_{0,1V}$ evaluated at +1.1 V vs. saturated mercurous sulfate electrode (MSE) vs. height for the six nanowires in (b) and (c) (red trace). Also plotted are the calculated resistance change caused by the constriction in the wire diameter (green trace) and the expected depression in p from 0.38 to 0.0 (blue trace) as well as the sum of these two contributions (black trace). Reproduced with permission from *Nano Letters*, 2008, **8**, 3017–3022. Copyright 2008 American Chemical Society.¹¹⁵

observations, we believe a new dissipation mechanism operates at nanowire surfaces. One candidate mechanism is the infiltration of the oxide into grain boundaries at wire surfaces which can directly impact the value of R —the reflection coefficient at grain boundaries—adding to the enhanced resistance caused by the oxide at the surface of the nanowire by a depression in p .

The electrical behavior of bismuth (Bi) nanowires is considerably more complex due to its small effective mass, large mean free path, and small charge carrier density and Bi nanowires continue to be the subject of intensive study.^{116–121} Bi nanowires are expected to show an extraordinary size dependence^{118,119} characterized by a transition from metallic to semiconducting behavior at a critical dimension of 50 nm as a consequence of a quantum-confinement-induced semimetal–semiconductor transition.¹²² We have so far studied two relatively large Bi nanowires with dimensions of 96 × 290 nm ($\rho_{300K} = 359 \Omega \text{ cm}$) and 260 × 650 nm ($\rho_{300K} = 654 \Omega \text{ cm}$). The measured room temperature resistivities of these nanowires (ρ_{300K}) were within the range of values measured previously^{6,123} and both showed monotonic thermally activated electrical conduction characteristic of semiconducting nanowires in spite of the fact that both were much larger than the 50 nm dimension above which bulk-like, metallic behavior is expected. The persistence of semiconducting behavior for bismuth nanowires with dimensions above 50 nm has been reported by Chiu and Shih¹²³ and non-monotonic resistivity temperature behavior has also been reported by Cornelius, Heremans and co-workers^{119,124,125} due to finite grain sizes.

Lead telluride nanowires

(a) Electrochemistry of PbTe nanowire synthesis

A strength of the LPNE method is that nanowires are formed from electrodeposited material. In principle, this opens the door to the synthesis of nanowires composed of a wide variety of functional metal oxides, semiconductors, and polymers. Our first foray into nonmetallic nanowire growth has involved the preparation of nanowires composed of lead telluride (PbTe), a material that is of interest because of its desirable thermoelectric properties.^{126–133}

The electrodeposition of PbTe is considerably more challenging than the growth of metal nanowires because the Pb : Te stoichiometry is critically important in this process and elemental excesses of both Pb and Te can readily be produced in addition to PbTe, degrading the quality of the deposited material.

Previously, we have employed an electrodeposition–stripping method to produce nanowires composed of Bi₂Te₃^{28,29} and CdSe.²⁴ The strategy in electrodeposition–stripping is to use a negative-going potential scan to synthesize the compound of interest (PbTe) as well as a small excess of lead (or cadmium). Then, on a subsequent positive-going scan, the excess Pb (or Cd) is stripped from the deposit to produce stoichiometric PbTe (or CdSe). The electrodeposition of elemental Te (or Se) is also possible at negative potentials within the synthesis range and Te (or Se) is not selectively removed during the ensuing anodic scan so it is critically important to minimize the concentration of these precursor species to eliminate excess elemental Te or Se in the produced nanowires. In general, this is accomplished by using a large (≈ 100 -fold) stoichiometric excess of the metal relative to the chalcogenide.^{130,134}

In Fig. 12 we show cyclic voltammograms associated with the growth of PbTe nanowires using LPNE and a nickel edge electrode. Here the synthesis solution contained 83 mM Pb²⁺ and just 0.83 mM TeO₃²⁻. On the negative-going scan to -0.85 V vs. SCE, PbTe and elemental Pb were concurrently electrodeposited and the excess lead is stripped from this deposit on the ensuing positive-going scan. The deposition

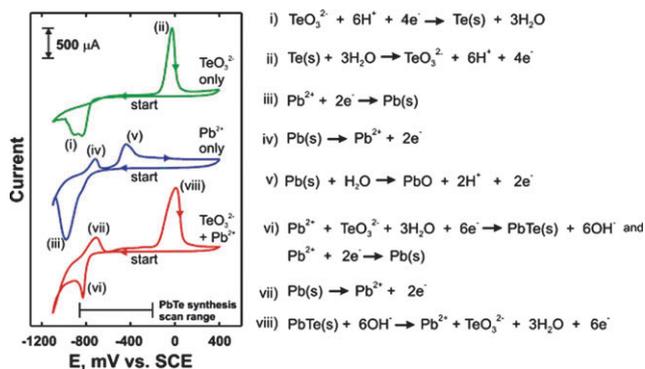


Fig. 12 Cyclic voltammograms (50 mV s^{-1}) for the electrodeposition of tellurium (top, green, $[\text{TeO}_3^{2-}] = 0.83 \text{ mM}$), lead (middle, blue, $[\text{Pb}^{2+}] = 83 \text{ mM}$) and lead telluride (bottom, red, $[\text{TeO}_3^{2-}] = 0.83 \text{ mM}$ and $[\text{Pb}^{2+}] = 83 \text{ mM}$) at $\text{pH} = 10$ in aqueous solution. The chemical reactions corresponding to the voltammetric waves are labeled as well. Reproduced with permission from *Nano Letters*, 2008, **8**, 2447–2451. Copyright 2008 American Chemical Society.³⁷

of elemental Te is suppressed because of the very low concentration ratio (1 : 100) of TeO_3^{2-} to Pb^{2+} . The positive limit of -0.2 V is selected to enable the quantitative removal of elemental lead without affecting the PbTe which is itself stripped at ≈ 0 V vs. SCE (Fig. 12, red curve).

(b) Structural and composition characterization of PbTe nanowires

The characterization of nanowires composed of compounds presents all of the issues that are encountered for metal

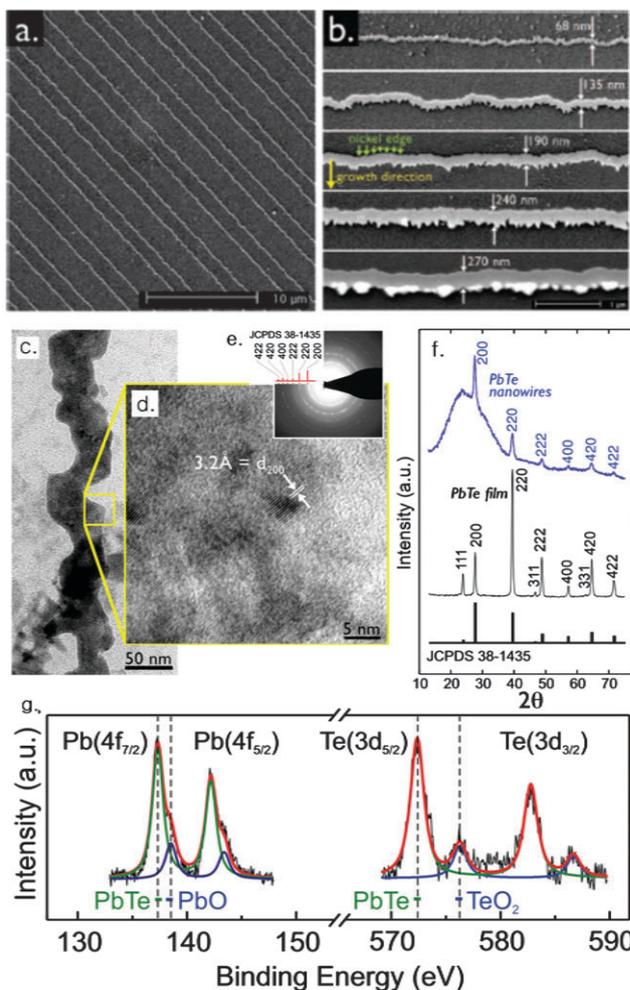


Fig. 13 Characterization of PbTe nanowires synthesized by LPNE. (a) SEM image of a PbTe nanowire array in which the lateral dimensions of the nanowires are 20 nm (h) \times 135 nm (w). (b) SEM images of individual PbTe nanowires with thicknesses of 20 nm and widths of 60 – 300 nm (from top to bottom). (c) TEM image of a PbTe nanowire with dimensions of 20 nm (h) \times 45 nm (w). (d) High-resolution TEM image. (e) Selected area electron diffraction (SAED) powder pattern for PbTe nanowires showing the assignment of six reflections to fcc PbTe (JCPDS 38-1435). (f) GIXRD patterns for an array of PbTe nanowires with dimensions of 60 nm (h) \times 200 nm (w) (blue) and an electrodeposited PbTe film of $\approx 75 \text{ nm}$ in thickness (black). (g) Narrow scan X-ray photoelectron spectra acquired for an array of PbTe nanowires showing Pb(4f) and Te(3d) regions. Reference binding energies for PbTe, PbO, and TeO₂ are indicated at the bottom. Reproduced with permission from *Nano Letters*, 2008, **8**, 2447–2451. Copyright 2008 American Chemical Society.³⁷

nanowires, including determination/verification of the bulk crystal structure, the detection and characterization of surface oxides, the measurement of the grain size, structure, and preferred orientation if any. New challenges involve the greater chemical and structural phase space, and the issue of stoichiometric excesses or deficiencies either within the bulk of the material or at wire surfaces.

A typical SEM image (Fig. 13a) of an array of PbTe nanowires captures a feature that is often seen for LPNE growth of linear wire arrays—the presence of two slightly different interwire spacings. This effect is caused by the fact that etching of the nickel layer reduces the interwire spacing in the direction of nickel removal. This asymmetry provides a way to quickly determine the growth direction for nanowires which is always towards the larger of the two interwire spacings. In high resolution SEM images (Fig. 13b), the edge of the nanowire that coincides with its growth direction is usually indicated by a greater edge roughness. This is apparent in Fig. 13b, for example, where the growth direction for all nanowires is down. As the nanowire width grows to the edge of the trench and fills it, the height dimension of the nanowire is no longer controlled and taller wire regions are produced along one edge (Fig. 13b, bottom). Images such as these reveal the depth of the trench and allow for the adjustment of this important parameter. Collectively, these SEM images clearly show that the cyclic electrodeposition–stripping method produces dense, continuous nanowires of PbTe that are free of breaks for hundreds of microns (Fig. 13a and b).

By controlling the number of scans, the width of PbTe nanowires can be adjusted from 60 nm to 400 nm (Fig. 13b and 14a). The height of PbTe nanowires is controllable using the thickness of the nickel layer deposited in step 1 of the LPNE process, just as with metal nanowires (Fig. 14b).

A TEM image of a PbTe nanowire ≈ 45 nm in width and 20 nm in height is shown in Fig. 13c. TEM images at higher magnification (Fig. 13d) permit the grain size to be directly measured and lattice fringe spacings can be measured to verify a particular crystal structure for the material. The image of Fig. 13d, for example, demonstrates good crystallinity by showing clear lattice fringes arrayed along the [200] direction with a d -spacing of 0.32 nm.¹³⁵ The existence of a crystallographically preferred growth direction can also be detected in data of this type, but this is not observed for PbTe. Selected

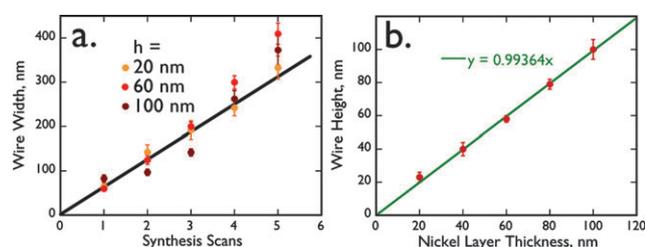


Fig. 14 (a) PbTe nanowire width versus the number of synthesis scans employed for electrodeposition. Data are shown for three wire thickness values of 20 (orange), 60 (red), and 100 nm (wine). (b) Relationship of PbTe wire height to thickness of nickel layer. Reproduced with permission from *Nano Letters*, 2008, 8, 2447–2451. Copyright 2008 American Chemical Society.³⁷

area electron diffraction (SAED) converts TEM images with lattice resolution into diffraction patterns. The SAED pattern in Fig. 13e shows six diffraction rings that can be assigned to a single phase of PbTe—namely face-center cubic (fcc) PbTe (diffraction file number JCPDS 38-1435).

The quality of X-ray powder diffraction (XRD) patterns far exceeds that available from SAED in part because XRD data is derived from a much larger total quantity of material. XRD patterns for PbTe nanowires (Fig. 13f, blue trace) were collected for an array of PbTe nanowires deposited at 2 μ m interwire pitch, resembling the gold nanowire array shown in Fig. 9a. As shown in Fig. 9b, an incident angle below the critical angle is used to achieve total external reflection of the X-rays from the silicon surface thereby maximizing the signal-to-noise ratio for the nanowires deposited on top. This incident angle is 0.3° in Fig. 13f.^{136,137} Diffraction peaks assignable to cubic PbTe (JCPDS 38-1435) are observed with high signal-to-noise. We routinely carry out the electro-deposition of the material of interest on a thin evaporated nickel layer for purposes of comparison to the LPNE nanowires (Fig. 13f, middle). In the case of PbTe, this thin film shows evidence of preferential texturing along [220]. If the contribution of lattice strain can be ignored, the Scherrer equation provides a means for determining the average grain size from the X-ray line width. When this analysis is applied to the XRD data for PbTe nanowires a mean grain size of 10–20 nm is obtained.

These XRD and TEM data provide no information on the chemical composition of nanowire surfaces where deviations from the bulk nanowire composition can be expected. X-Ray photoelectronic spectroscopy (XPS) is a powerful tool for probing surface chemical composition and we have been fortunate to carry out XPS analysis of nanowires in a collaboration with Prof. John Hemminger and his research group at UCI. Typical narrow scan XP spectra of PbTe nanowires that were exposed to air for a few minutes are shown in Fig. 13g. For both Pb(4f), and Te(3d) regions, two pairs of doublets are seen—the more intense doublets are derived from PbTe, while the weaker doublets can be assigned to oxides of lead and tellurium with estimated thicknesses of 0.56 nm for PbO and 0.37 nm TeO₂, respectively. From this result we conclude that air oxidation of PbTe nanowires is rapid at room temperature.

(c) Suspended PbTe nanowires

To measure the thermal properties of nanowires composed of PbTe and other materials, these nanowires must be thermally isolated from the surfaces on which they are supported. To accomplish this, nanowires must be suspended across air or vacuum gaps.^{138,139} We have developed a method called photoresist-bottomed LPNE (called PB-LPNE) in order to achieve this suspension for arrays of PbTe nanowires. PB-LPNE (Fig. 15a, b) allows the suspension of 25 μ m nanowire sections 2 μ m above a silicon surface between microfabricated photoresist bumps. The details of the PB-LPNE procedure are described elsewhere.³⁷ This process (Fig. 15c) departs from the baseline LPNE process (Fig. 1) by starting with a glass or silicon surface on which a photoresist (PR) layer 1–2 μ m has been deposited (Fig. 15c). At the end of the PB-LPNE process,

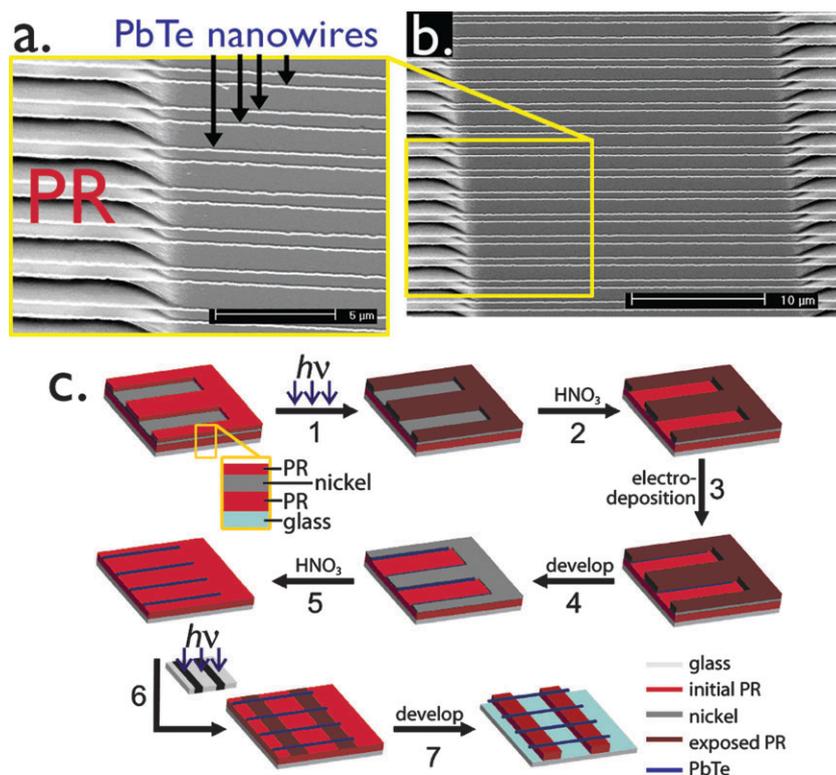


Fig. 15 Synthesis of air-suspended PbTe nanowires. (a, b) SEM images of suspended PbTe nanowire arrays at 2 μm pitch density. The air gap between the PbTe nanowires and the glass surface is $\approx 2 \mu\text{m}$ in this case. (c) Process flow for PB-LPNE commencing, at upper left, with step 4 of the “baseline” LPNE process (Fig. 1). Unique to PB-LPNE is the PR layer interposed between the nickel and glass. Reproduced with permission from *Nano Letters*, 2008, **8**, 2447–2451. Copyright 2008 American Chemical Society.³⁷

this PR layer is patterned to produce a series of linear, periodic supports between which nanowires are suspended.

(d) Electrical conductivity of PdTe nanowires

The air instability of PbTe nanowires demonstrated by the XPS spectra of Fig. 13g presents a barrier to the electrical characterization of these nanowires: How can their electrical properties be evaluated when an air exposure of a few minutes causes the formation of an insulating surface oxide layer? This

duration is simply too short to permit the preparation by thermal evaporation of electrical contacts.

A solution to this problem is depicted in Fig. 16a. Since in the LPNE method, PbTe nanowires are grown on nickel nanoband electrodes, an intimate electrical contact is formed at the nickel–PbTe interface along the entire axis of the nanowire. Therefore, after the nanowire is deposited and the photoresist has been removed, this sacrificial nickel layer can be patterned to form the electrical contacts necessary to make

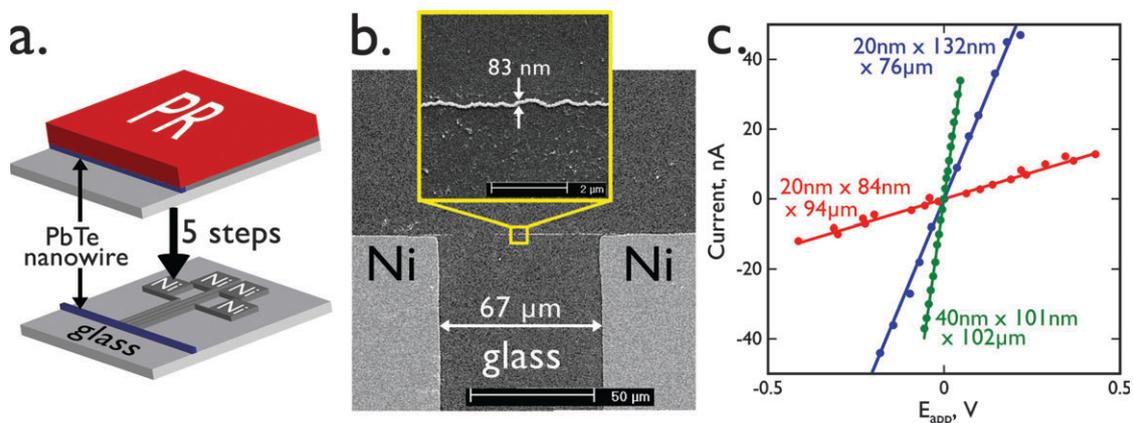


Fig. 16 (a) Schematic showing that the patterned nickel edge used for nanowire growth can later be patterned and used for a four-point electrical measurement of the wire resistance. (b) SEM image of the inner two nickel electrodes and a PbTe nanowire. The electrically isolated wire length in this instance was 94 μm , greater than the interelectrode distance of 67 μm . (c) Ohmic current *versus* voltage plots for three PbTe nanowires with dimensions as indicated. Reproduced with permission from *Nano Letters*, 2008, **8**, 2447–2451 Copyright 2008 American Chemical Society.³⁷

high quality, four-point measurements of the nanowire resistance. The patterning of the nickel layer can be carried out using photolithography. The central portion of such a device is shown in the SEM image of Fig. 16b. Using devices such as these, I - V curves for three PbTe nanowires were acquired (Fig. 15c), yielding conductivities ranging from 0.70×10^4 to $1.8 \times 10^4 \text{ S m}^{-1}$. This value is in the range of conductivity values of bulk PbTe in the literature.^{135,140,141} This approach is not limited to PbTe and we expect it to be useful for the electrical characterization of a variety of other air-reactive nanowire materials.

Conclusions

Lithographically patterned nanowire electrodeposition (LPNE) is a new tool for the synthesis of nanowires on surfaces. LPNE leverages photolithography to control the position and path of nanowires and electrochemistry to synthesize them. Nanowires may be produced in parallel over wafer scale distances, and nanowires can be electrically continuous for centimetres, but lateral nanowire dimensions are not constrained by the diffraction limit: wire widths are controlled by the electrodeposition parameters, and the wire height by the template prepared by photolithography.

LPNE makes it possible to pattern nanowires faster, and at lower cost, than is possible by any other currently available method to our knowledge. This cost efficiency exists as a consequence of the fact that nanowires are produced over large, wafer-scale regions in parallel. The competing method of electron beam lithography requires nanowires to be serially written in photoresist using an electron beam, expending far greater time, proportional to the length of the nanowires to be produced, and requiring an expensive electron beam writer. As a specific example, the fabrication by LPNE of the nanowire array shown in Fig. 9a, consisting of $20 \text{ nm} \times 200 \text{ nm}$ nanowires each 1 cm in length and spaced laterally by $2 \mu\text{m}$ (a total nanowire length of 50 m!) required approximately 6 h. Approximately 500 h would be required to produce a similar array using an electron beam writer operating at 10 cm h^{-1} . Is the time efficiency of LPNE economically offset by the demands for electrical power of the method? No, this is not the case because of the minute amounts of material that are deposited. Referring again to the nanowire array of Fig. 9a, a total of just 6 mC (or 6 mA for one second) would be required to produce this gold nanowire array. LPNE opens the door to the use of nanowires in integrated circuits, in chemical sensors, and in optical devices such as diffraction gratings where it has not been practical to employ nanowires up until now.

Because the gamut of materials accessible using electrodeposition is enormous, ranging from metal oxides, to polymers, to semiconducting compounds, to conductive charge transfer complexes in addition to metals, the potential for LPNE to produce nanowires with unique and useful properties is unbounded.

A central challenge for future work is control of the grain size. LPNE produces polycrystalline, not single crystalline, nanowires. Methods must be developed for adjusting the grain size without altering their lateral dimensions or degrading the

wire dimensional uniformity. A long term goal of this work is to obtain single crystalline metal and semiconductor nanowires with lengths in the millimetre range.

Acknowledgements

In addition to Erik Menke who invented LPNE, and the authors of this paper who have been central to its development, a larger group of talented and dedicated students have made valuable contributions, including: Aleix G. Güell, Jung Yun Kim, Sheng-Chin Kung, Michael Thompson, David Taggart, Fan Yang, and Li-Mei Yang. Crucial to the success of this work have been collaborations with Prof. John C. Hemminger, Matt Brown, Prof. Eric Potma and Hyunmin Kim. This research has been financially supported by the National Science Foundation (grants: CHE-0641169, DMR-0654055), the Petroleum Research Fund of the American Chemical Society (grant: 46815-AC10), and the UCI School of Physical Sciences Center for Solar Energy.

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